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DATE: 4/13/04
TO: Examiner N. Levin
COMPANY: USPTO
FROM: Gregory Suh
S/N: 10/062,044
PAGES: 7 (including this page)

Examiner N. Levin:

Accompanying this cover letter are 1449 forms of Information Disclosure Statements that Applicants have previously submitted for the above-identified patent application but which Examiner has not yet made of record. These Information Disclosure Statements list and provide copies of several additional references for the Examiner's consideration. The Examiner is requested to make these documents of record.

Regards,

Gregory Suh

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Application Number	10/062,044
				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2825
				Examiner Name	Naum B. Levin
Sheet	1	of	1	Attorney Docket Number	SPLX.P0093

RELATED U.S. PATENT APPLICATIONS					
Examiner* Initials	Cite No.	U.S. Patent Application Serial Number	Name of Patentee or Applicant of Cited Document	Date of Filing MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	10/062,017	Steven Teig & Asmus Hetzel	01-31-02	
	2.	10/061,459	Steven Teig & Asmuz Hetzel	01-31-02	
	3.	10/062,014	Steven Teig & Asmus Hetzel	01-31-02	
	4.	10/066,264	Steven Teig & Asmuz Hetzel	01-31-02	
	5.	10/066,188	Steven Teig & Asmus Hetzel	01-31-02	
	6.	10/062,992	Steven Teig & Asmus Hetzel	01-31-02	
	7.	10/061,474	Steven Teig & Asmuz Hetzel	01-31-02	
	8.	10/061,719	Steven Teig & Asmus Hetzel	01-31-02	
	9.	10/066,456	Steven Teig & Asmus Hetzel	01-31-02	
	10.	10/062,993	Steven Teig & Asmus Hetzel	01-31-02	
	11.	10/062,047	Steven Teig & Asmuz Hetzel	01-31-02	

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Sheet	2	of	2	Attorney Docket Number	SPLX.P0093

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	-5
	12.	D. Jongeneel, R. Otten, Y. Watanabe and R. K. Brayton, Area and Search Space Control for Technology Mapping, 37 th Design Automation Conference, 86-91, 2000.	
	13.	Henrik Reif Andersen, An Introduction to Binary Decision Diagrams, October 1997 (minor revisions April 1998), 36 pp.	
	14.	Jerry Burch and David Long, Efficient Boolean Function Matching, Proc. ICCAD 1992, 408-411.	
	15.	John Fishburn, A Depth-Decreasing Heuristic for Combinational Logic; or How to Convert Ripple-Carry Adder into a Carry-Lookahead Adder or Anything In-Between. Proceedings of the 27 th Design Automation Conference, 361-364, 1990.	
	16.	Kamal Chaudhary and Massoud Pedram, A Near Optimal Algorithm for Technology Mapping Minimizing Area under Delay Constraints, Proceedings of the 29 th Design Automation Conference, 492-498, 1992.	
	17.	Kurt Keutzer, DAGON: Technology Binding and Local Optimization by DAG Matching, Proceedings of the 24 th Design Automation Conference, 341-347, 1987.	
	18.	Randal Bryant, Symbolic Boolean Manipulation with Ordered Binary Decision Diagrams, CMU CS Tech Report CMU-CS-92-160.	
	19.	Uwe Hinsberger and Reiner Kolla, Boolean Matching for Large Libraries, Proceedings of the 35 th Design Automation Conference, 206-211, June 1998.	
	20.	Yuji Kukimoto, Robert K. Brayton, and Prashant Sawkar, Delay-Optimal Technology Mapping by DAG Covering, Dept. of Electrical Engineering and Computer Science, University of California, Berkeley, Strategic CAD Laboratories, Intel Corp., October 1997.	
	21.	Zbigniew J. Czech, et al., An Optimal Algorithm for Generating Minimal Perfect Hashing Functions, Information Processing Letters, 43(5): 257-264, October 1992.	

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			Group Art Unit	2825	
			Examiner Name	Naum B Levin	
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U.S. PATENT DOCUMENTS					
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	1.	6,134,705	10-17-2000	Pedersen et al	
	2.	6,102,964	08-15-2000	Tse et al	
	3.	6,473,884	10-29-2002	Ganai et al	
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	12.	6,546,539	04-08-2003	Lu et al	

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			Group Art Unit	2825	
			Examiner Name	N. Levin	
			Attorney Docket Number	SPLX.P0093	
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U.S. PATENT DOCUMENTS						
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	1.	2002/0157063	A1	10-24-2002	Besson	
	2.	2002/0178432	A1	11-28-2002	Kim et al.	
	3.	2003/0145288	A1	07-31-2003	Wang et al.	
	4.	4,703,435		10-27-1987	Darringer et al.	
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	16.	6,334,205		12-25-2001	Iyer et al.	
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	20.	6,446,240	B1	09-03-2002	Iyer et al.	
	21.	6,453,447	B1	09-17-2002	Gardner et al.	

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U.S. PATENT DOCUMENTS					
22.	6,470,478	B1	10-22-2002	Bargh et al.	
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32.	6,618,835	B1	09-09-2003	Garlapati et al.	

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NON PATENT LITERATURE DOCUMENTS			
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	33.	NN78055443, "Automatic Remap", IBM Technical Disclosure Bulletin, Vol. 20, No. 12, May 1978, pp. 5443-5445 (5 pages).	
	34.	NN9411291, "Design of Portable Library using Parameterized Cells", IBM Technical Disclosure Bulletin, Vol. 37, No. 11, pp. 291-292 (4 pages).	
	35.	Markovic et al., "FPGA to ASIC Conversion Design Methodology with the Support for Fast Retargeting to Different CMOS Implementation Technologies", Proceedings of 2002 22 nd International Conference on Microelectronics, Vol. 2, 14 May 2000, pp. 703-706.	
	36.	Ruiz et al., "Design and Prototyping of DSP Custom Circuits Based on a Library of Arithmetic Components", Vol. 1, 9 November 1997, pp. 191-196.	
	37.	Tamiya, Y., "Delay Estimation for Technology Independent Synthesis", 1997 Proceedings of the ASP-DAC '97, Asia and South Pacific Design Automation Conference, 28 January 1997, pp. 31-36.	
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